



**AOD4185/AOI4185**

**P-Channel Enhancement Mode Field Effect Transistor**

**General Description**

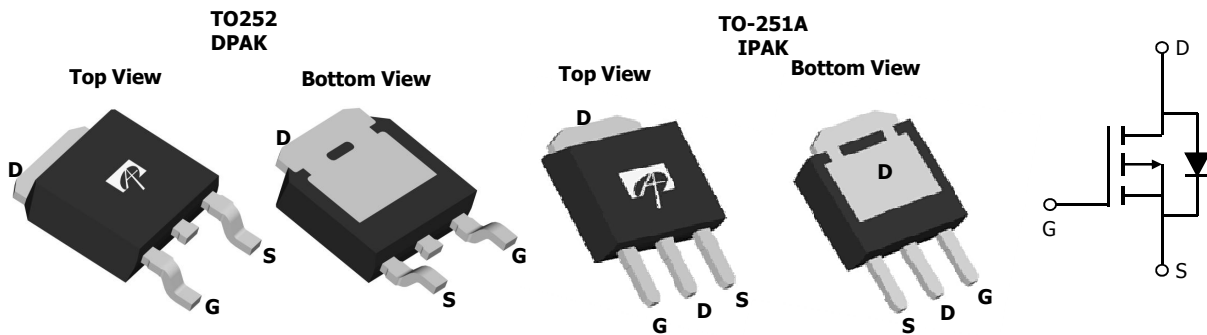
The AOD4185/AOI4185 uses advanced trench technology to provide excellent  $R_{DS(ON)}$  and low gate charge. With the excellent thermal resistance of the DPAK/IPAK package, this device is well suited for high current applications.

- RoHS Compliant
- Halogen Free\*

**Features**

$V_{DS}$  (V) = -40V  
 $I_D$  = -40A ( $V_{GS} = -10V$ )  
 $R_{DS(ON)} < 15m\Omega$  ( $V_{GS} = -10V$ )  
 $R_{DS(ON)} < 20m\Omega$  ( $V_{GS} = -4.5V$ )

**100% UIS Tested!**  
**100% Rg Tested!**



**Absolute Maximum Ratings  $T_C=25^\circ C$  unless otherwise noted**

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	$V_{DS}$	-40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>B,H</sup>	$I_D$	$T_C=25^\circ C$	A
		$T_C=100^\circ C$	
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	-115	A
Avalanche Current <sup>C</sup>	$I_{AR}$	-42	A
Repetitive avalanche energy $L=0.1mH$ <sup>C</sup>	$E_{AR}$	88	mJ
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ C$	W
		$T_C=100^\circ C$	
Power Dissipation <sup>A</sup>	$P_{DSM}$	$T_A=25^\circ C$	W
		$T_A=70^\circ C$	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	$^\circ C$

**Thermal Characteristics**

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A,G</sup>	$R_{\theta JA}$	15	20	$^\circ C/W$
$t \leq 10s$				
Maximum Junction-to-Ambient <sup>A,G</sup>	$R_{\theta JC}$	2	2.4	$^\circ C/W$
Steady-State				
Maximum Junction-to-Case <sup>D,F</sup>				

Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$I_D=-250\mu\text{A}$ , $V_{GS}=0\text{V}$	-40			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=-40\text{V}$ , $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			-1	$\mu\text{A}$
					-5	
$I_{GSS}$	Gate-Body leakage current	$V_{DS}=0\text{V}$ , $V_{GS}=\pm 20\text{V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$ , $I_D=-250\mu\text{A}$	-1.7	-1.9	-3	V
$I_{D(ON)}$	On state drain current	$V_{GS}=-10\text{V}$ , $V_{DS}=-5\text{V}$	-115			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=-10\text{V}$ , $I_D=-20\text{A}$ $T_J=125^\circ\text{C}$		12.5	15	m $\Omega$
				19	23	
		$V_{GS}=-4.5\text{V}$ , $I_D=-15\text{A}$		16	20	
$g_{FS}$	Forward Transconductance	$V_{DS}=-5\text{V}$ , $I_D=-20\text{A}$		50		S
$V_{SD}$	Diode Forward Voltage	$I_S=-1\text{A}$ , $V_{GS}=0\text{V}$		-0.72	-1	V
$I_S$	Maximum Body-Diode Continuous Current				-20	A
<b>DYNAMIC PARAMETERS</b>						
$C_{iss}$	Input Capacitance	$V_{GS}=0\text{V}$ , $V_{DS}=-20\text{V}$ , $f=1\text{MHz}$		2550		pF
$C_{oss}$	Output Capacitance			280		pF
$C_{rss}$	Reverse Transfer Capacitance			190		pF
$R_g$	Gate resistance	$V_{GS}=0\text{V}$ , $V_{DS}=0\text{V}$ , $f=1\text{MHz}$	2.5	4	6	$\Omega$
<b>SWITCHING PARAMETERS</b>						
$Q_g(-10\text{V})$	Total Gate Charge	$V_{GS}=-10\text{V}$ , $V_{DS}=-20\text{V}$ , $I_D=-20\text{A}$		42	55	nC
$Q_g(-4.5\text{V})$	Total Gate Charge			18.6		
$Q_{gs}$	Gate Source Charge			7		nC
$Q_{gd}$	Gate Drain Charge			8.6		nC
$t_{D(on)}$	Turn-On Delay Time			9.4		ns
$t_r$	Turn-On Rise Time	$V_{GS}=-10\text{V}$ , $V_{DS}=-20\text{V}$ , $R_L=1\Omega$ , $R_{GEN}=3\Omega$		20		ns
$t_{D(off)}$	Turn-Off Delay Time			55		ns
$t_f$	Turn-Off Fall Time			30		ns
$t_{rr}$	Body Diode Reverse Recovery Time	$I_F=-20\text{A}$ , $dI/dt=100\text{A}/\mu\text{s}$		38	49	ns
$Q_{rr}$	Body Diode Reverse Recovery Charge	$I_F=-20\text{A}$ , $dI/dt=100\text{A}/\mu\text{s}$		47		nC

A: The value of  $R_{\theta JA}$  is measured with the device in a still air environment with  $T_A=25^\circ\text{C}$ . The power dissipation  $P_{DSM}$  and current rating  $I_{DSM}$  are based on  $T_{J(MAX)}=150^\circ\text{C}$ , using steady state junction-to-ambient thermal resistance.

B: The power dissipation  $P_D$  is based on  $T_{J(MAX)}=175^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature  $T_{J(MAX)}=175^\circ\text{C}$ .

D: The  $R_{\theta JA}$  is the sum of the thermal impedance from junction to case  $R_{\theta JC}$  and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using  $<300\mu\text{s}$  pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of  $T_{J(MAX)}=175^\circ\text{C}$ . The SOA curve provides a single pulse rating.

G: These tests are performed with the device mounted on a 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ .

H: The maximum current rating is limited by bond-wires.

\*This device is guaranteed green after data code 8X11 (Sep 1<sup>ST</sup> 2008).

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

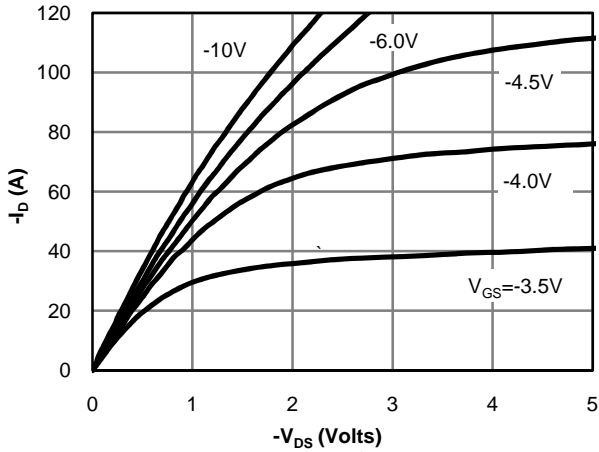


Figure 1: On-Region Characteristics

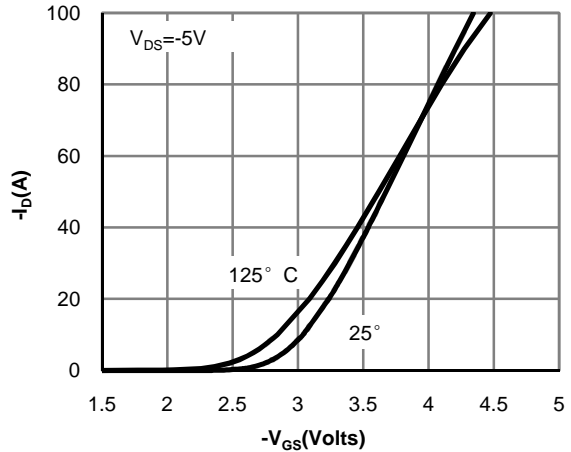


Figure 2: Transfer Characteristics

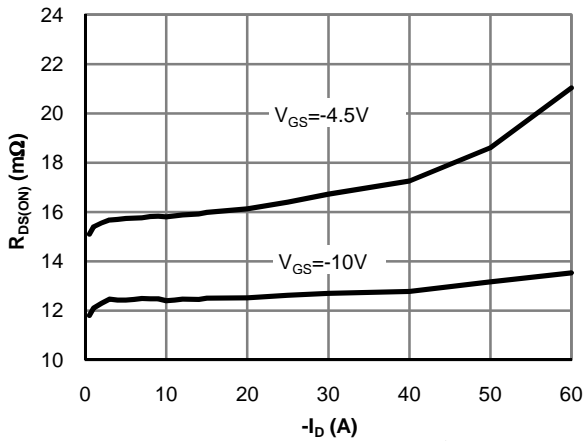


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

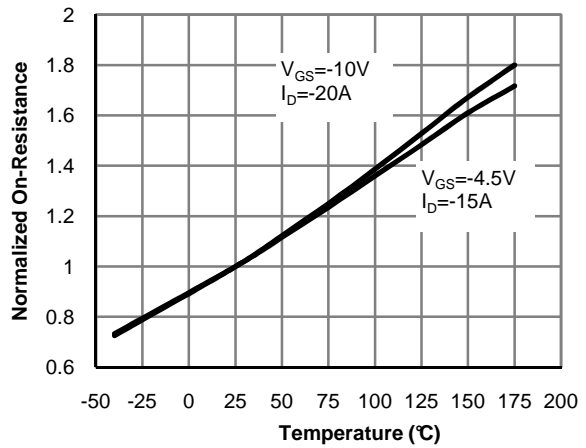


Figure 4: On-Resistance vs. Junction Temperature

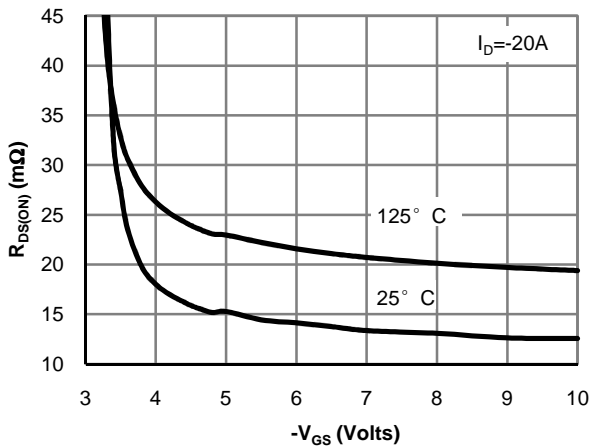


Figure 5: On-Resistance vs. Gate-Source Voltage

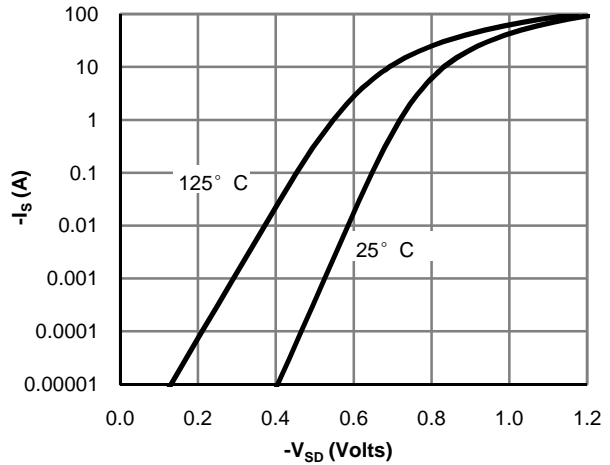


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

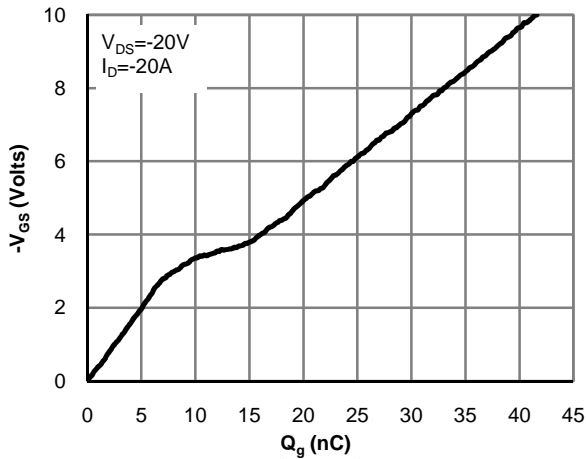


Figure 7: Gate-Charge Characteristics

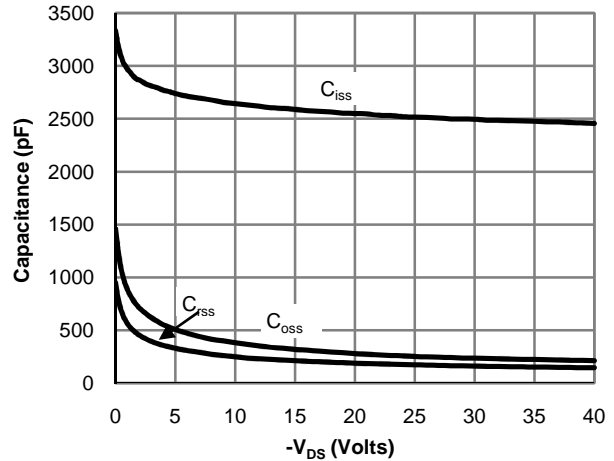


Figure 8: Capacitance Characteristics

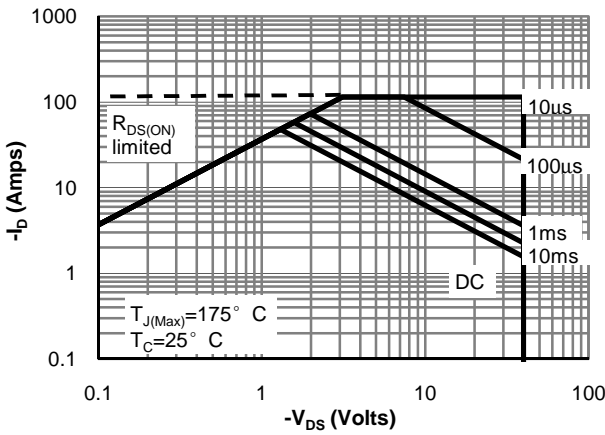


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

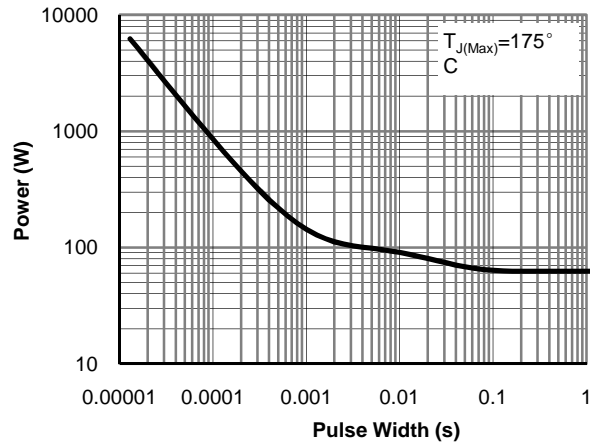


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

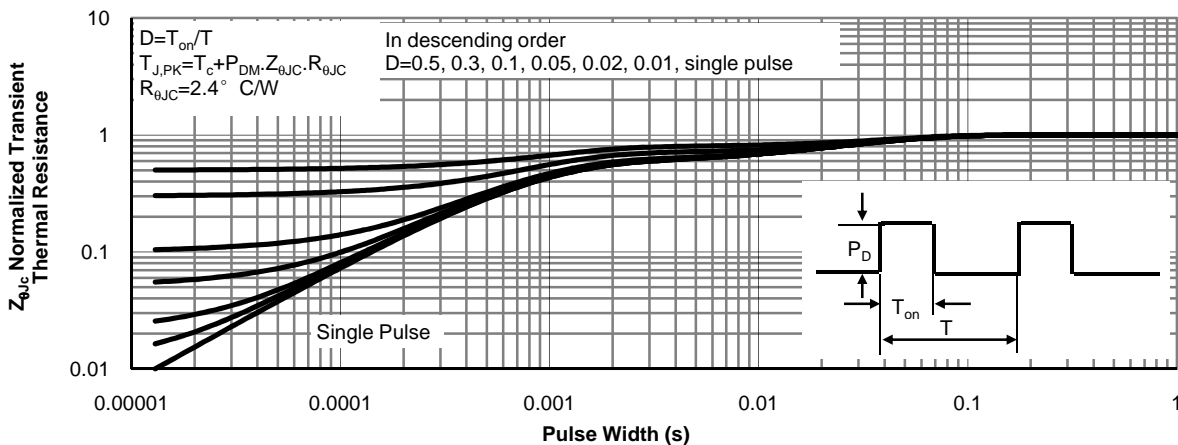


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

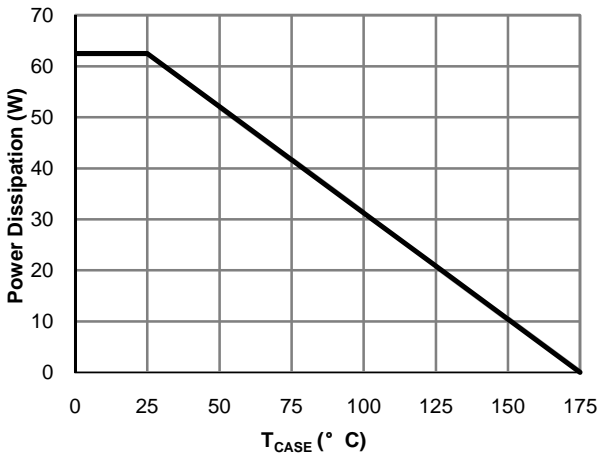


Figure 12: Power De-rating (Note B)

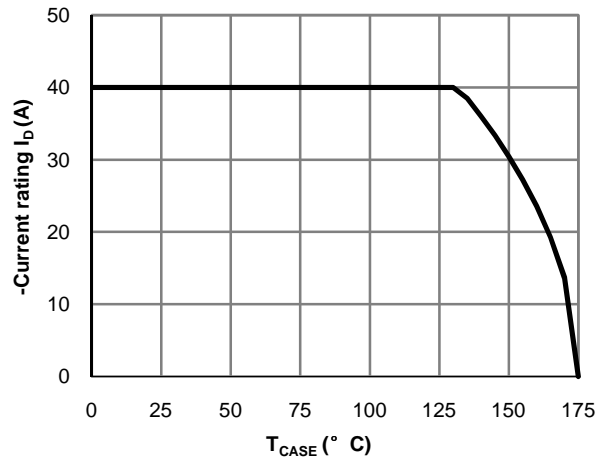


Figure 13: Current De-rating (Note B)

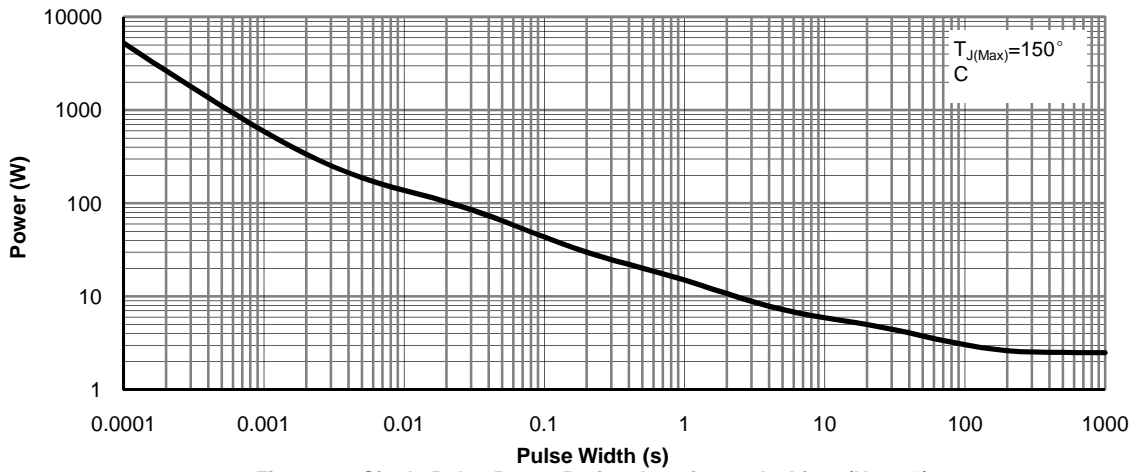


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note G)

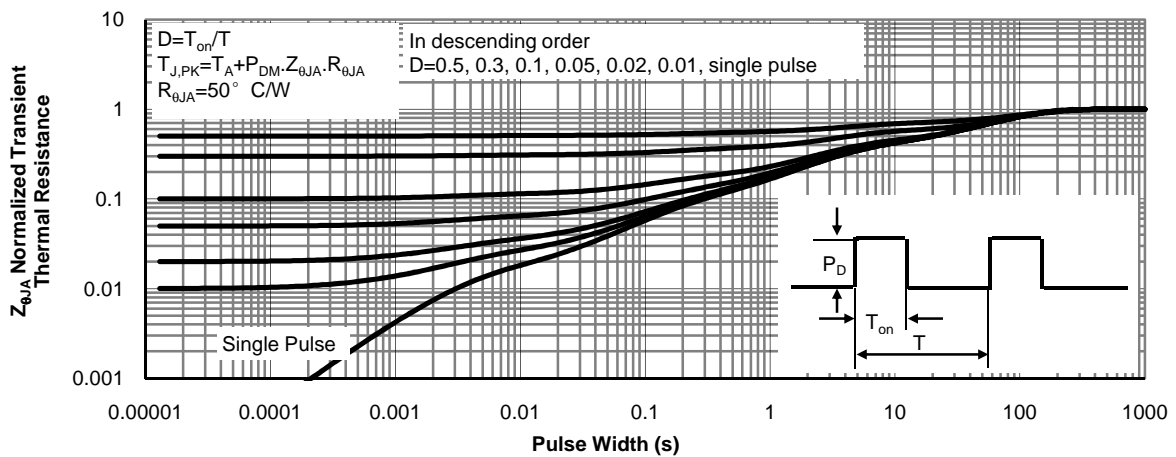
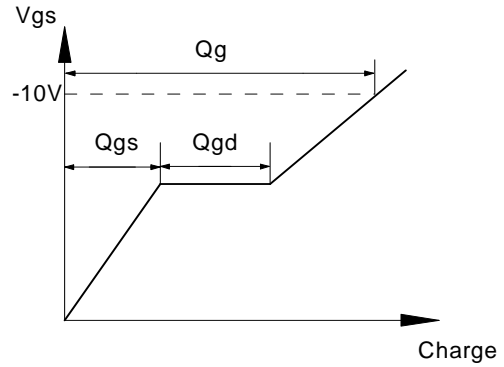
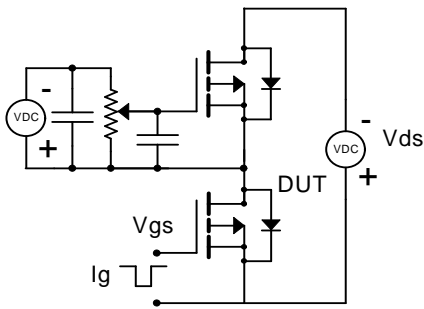
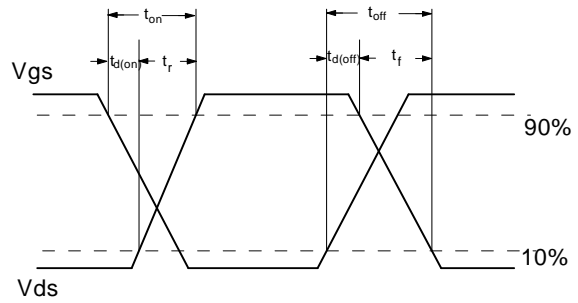
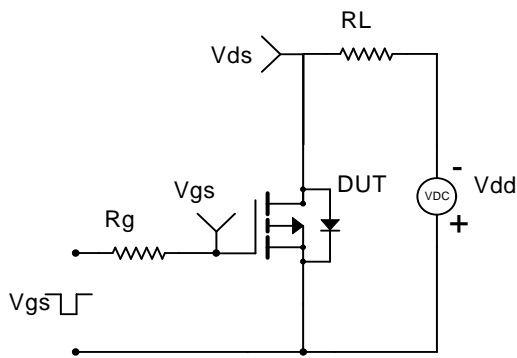


Figure 15: Normalized Maximum Transient Thermal Impedance (Note G)

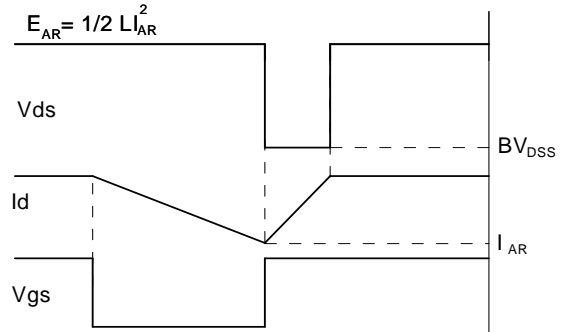
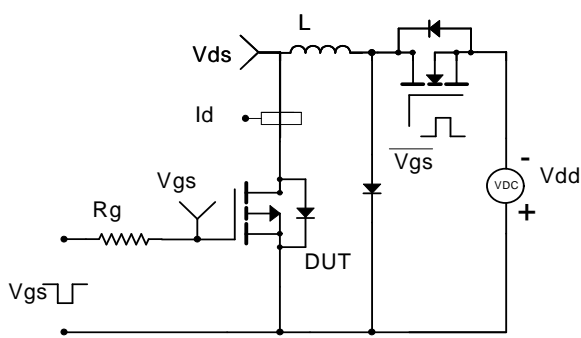
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

