



Ultra-small 17 mΩ 2.5 A Load Switch with Discharge

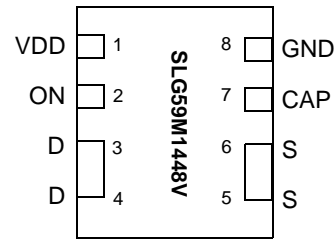
General Description

The SLG59M1448V is a 17 mΩ 2.5 A single-channel load switch that is able to switch 0.9 to 5 V power rails. The product is packaged in an ultra-small 1.0 x 1.6 mm package.

Features

- 1.0 x 1.6 x 0.55 mm STDFN 8L package (2 fused pins for drain and 2 fused pins for source)
- Logic level ON pin capable of supporting 0.85 V CMOS Logic
- User selectable ramp rate with external capacitor
- 17 mΩ RDS_{ON} while supporting 2.5 A
- Discharges load when off
- Two Over Current Protection Modes
 - Short Circuit Current Limit
 - Active Current Limit
- Over Temperature Protection
- Pb-Free / Halogen-Free / RoHS compliant
- Operating Temperature: -40 °C to 85°C
- Operating Voltage: 2.5 V to 5.5 V

Pin Configuration

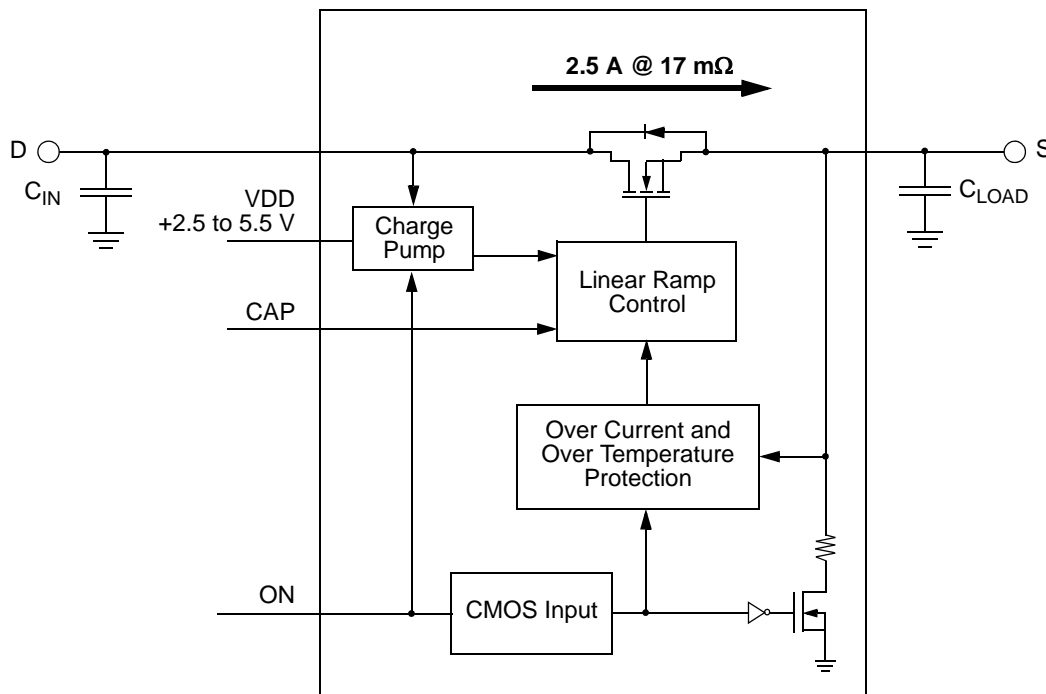


**8-pin STDFN
(Top View)**

Applications

- Notebook Power Rail Switching
- Tablet Power Rail Switching
- Smartphone Power Rail Switching

Block Diagram





Pin Description

| Pin # | Pin Name | Type | Pin Description |
|-------|----------|--------|--|
| 1 | VDD | PWR | VDD power for load switch control (2.5 V to 5.5 V) |
| 2 | ON | Input | Turns MOSFET ON (4 M Ω pull down resistor) CMOS input with VIL < 0.3 V, VIH > 0.85 V |
| 3 | D | MOSFET | Drain of Power MOSFET (fused with pin 4) |
| 4 | D | MOSFET | Drain of Power MOSFET (fused with pin 3) |
| 5 | S | MOSFET | Source of Power MOSFET (fused with pin 6) |
| 6 | S | MOSFET | Source of Power MOSFET (fused with pin 5) |
| 7 | CAP | Input | Capacitor for controlling power rail ramp rate |
| 8 | GND | GND | Ground |

Ordering Information

| Part Number | Type | Production Flow |
|---------------|--------------------------|-----------------------------|
| SLG59M1448V | STDFN 8L | Industrial, -40 °C to 85 °C |
| SLG59M1448VTR | STDFN 8L (Tape and Reel) | Industrial, -40 °C to 85 °C |



Absolute Maximum Ratings

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|----------------------------|-----------------------------------|--|------|------|------|------|
| V _{DD} | Power Supply | | -- | -- | 7 | V |
| T _S | Storage Temperature | | -65 | -- | 150 | °C |
| ESD _{HBM} | ESD Protection | Human Body Model | 8000 | -- | -- | V |
| MSL | Moisture Sensitivity Level | | 1 | | | |
| W _{DIS} | Package Power Dissipation | | -- | -- | 0.4 | W |
| MOSFET I _{DS(PK)} | Peak Current from Drain to Source | For no more than 1 ms with 1% duty cycle | -- | -- | 3.5 | A |

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

T_A = -40 °C to 85 °C (unless otherwise stated)

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|------------------------|--------------------------------------|--|---------------------------|------|-----------------|------|
| V _{DD} | Power Supply Voltage | -40 °C to 85 °C | 2.5 | -- | 5.5 | V |
| I _{DD} | Power Supply Current (PIN 1) | when OFF | -- | -- | 1 | μA |
| | | when ON, No C _{LOAD} | -- | 70 | 100 | μA |
| R _{DS(ON)} | Static Drain to Source ON Resistance | T _A 25°C @ 100 mA | -- | 17 | 19 | mΩ |
| | | T _A 70°C @ 100 mA | -- | 18.5 | 20 | mΩ |
| | | T _A 85°C @ 100 mA | -- | 22 | 24 | mΩ |
| I _{DS} | Operating Current | V _D = 1.0 V to 5.5 V | -- | -- | 2.5 | A |
| V _D | Drain Voltage | | 0.9 | -- | V _{DD} | V |
| T _{ON_Delay} | ON pin Delay Time | 50% ON to Ramp Begin | 0 | 300 | 500 | μs |
| T _{Total_ON} | Total Turn On Time | 50% ON to 90% V _S | Configurable ¹ | | | ms |
| | | Example: CAP (PIN 7) = 4 nF, V _{DD} = V _D = 5 V, C _{LOAD} = 10 μF, I _{DS} = 100 mA | -- | 1.96 | -- | ms |
| T _{SLEWRATE} | Slew Rate | 10% V _S to 90% V _S | Configurable ¹ | | | V/ms |
| | | Example: CAP (PIN 7) = 4 nF, V _{DD} = V _D = 5 V, C _{LOAD} = 10 μF, I _{DS} = 100 mA | -- | 3.0 | -- | V/ms |
| C _{LOAD} | Output Load Capacitance | C _{LOAD} connected from V _S to GND | -- | -- | 500 | μF |
| R _{DIS} | Discharge Resistance | | 100 | 150 | 300 | Ω |
| ON_V _{IH} | High Input Voltage on ON pin | | 0.85 | -- | V _{DD} | V |
| ON_V _{IL} | Low Input Voltage on ON pin | | -0.3 | 0 | 0.3 | V |
| I _{LIMIT} | Active Current Limit | MOSFET will automatically limit current when V _S > 250 mV | -- | 3.7 | -- | A |
| | Short Circuit Current Limit | MOSFET will automatically limit current when V _S < 250 mV | -- | 0.9 | -- | A |
| THERM _{ON} | Thermal shutoff turn-on temperature | | -- | 125 | -- | °C |
| THERM _{OFF} | Thermal shutoff turn-off temperature | | -- | 100 | -- | °C |
| THERM _{TIME} | Thermal shutoff time | | -- | -- | 1 | ms |
| T _{OFF_Delay} | OFF Delay Time | 50% ON to V _S Fall, V _{DD} = V _D = 5 V | -- | 8 | -- | μs |



Electrical Characteristics (continued)

$T_A = -40\text{ }^\circ\text{C}$ to $85\text{ }^\circ\text{C}$ (unless otherwise stated)

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|------------|-----------------|--|------|------|------|---------------|
| T_{FALL} | V_S Fall Time | 90% V_S to 10% V_S , $V_{DD} = V_D = 5\text{ V}$ | -- | 3.8 | -- | μs |

Notes:

1. Refer to table for configuration details.



SLG59M1448V Power-Up/Power-Down Sequence Considerations

To ensure glitch-free power-up under all conditions, apply V_{DD} first, followed by V_D after V_{DD} exceeds 1 V. Then allow V_D to reach 90% of its max value before toggling the ON pin from Low-to-High. Likewise, power-down in reverse order.

If V_{DD} and V_D need to be powered up simultaneously, glitching can be minimized by having a suitable load capacitor. A 10 μ F C_{LOAD} will prevent glitches for rise times of V_{DD} and V_D less than 2 ms.

If the ON pin is toggled HIGH before V_{DD} and V_D have reached their steady-state values, the IPS timing parameters may differ from datasheet specifications.

The slew rate of output V_S follows a linear ramp set by a capacitor connected to the CAP pin. A larger capacitor value at the CAP pin produces a slower ramp, reducing inrush current from capacitive loads.

SLG59M1448V Current Limiting

The SLG59M1448V has two modes of current limiting, differentiated by the output (Source pin) voltage.

1. Standard Current Limiting Mode (with Thermal Protection)

When $V(S) > 250$ mV, the output current is initially limited to the Active Current Limit specification given in the Electrical Characteristics table. The current limiting circuit is very fast and responds within a few micro-seconds to sudden loads. When overload is sensed, the current limiting circuit increases the FET resistance to keep the current from exceeding the Active Current Limit.

However, if an overload condition persists, the die temperature rise due to the increased FET resistance while at maximum current can activate Thermal Protection. If the die temperature exceeds the $THERM_{ON}$ specification, the FET is shut completely OFF, allowing the die to cool. When the die cools to the $THERM_{OFF}$ temperature, the FET is allowed to turn back on. This process may repeat as long as the overload condition is present.

2. Short Circuit Current Limiting Mode (with Thermal Protection)

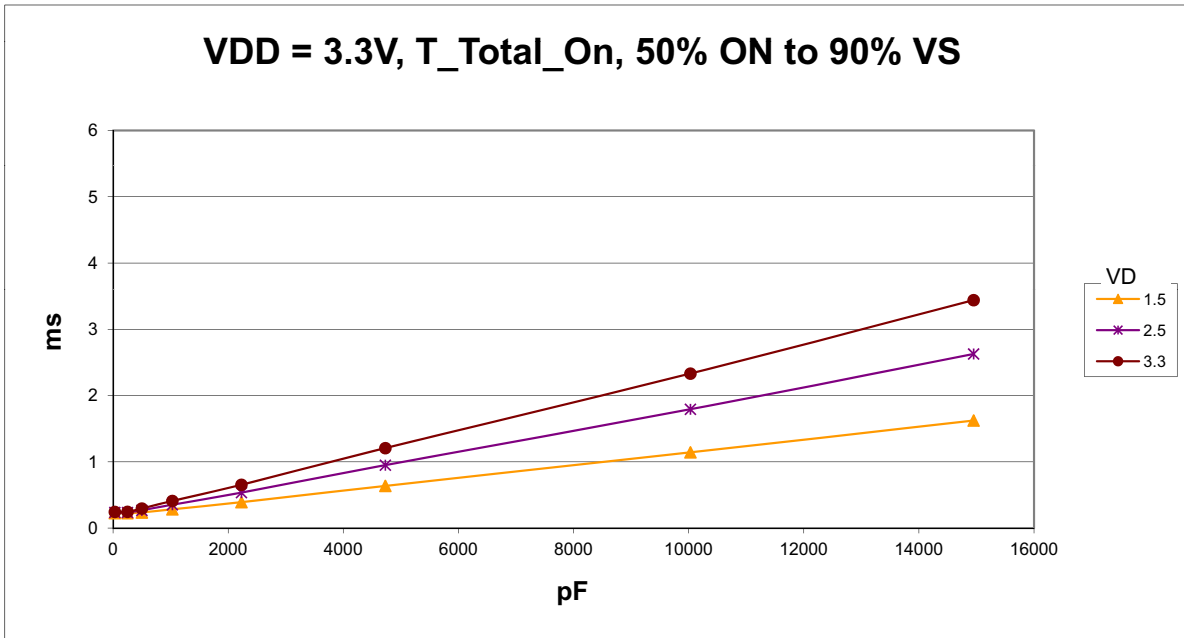
When $V(S) < 250$ mV (which is the case with a hard short, such as a solder bridge on the power rail), the current is limited to approximately 500 mA. Thermal Protection is also present, but since the Short Circuit Current Limit is much lower than Standard Current Limit, activation may only occur at higher ambient temperatures.

For more information on Silego GreenFET3 integrated power switch features, please visit our [Application Notes](#) page at our website and see [App Note "AN-1068 GreenFET3 Integrated Power Switch Basics"](#).



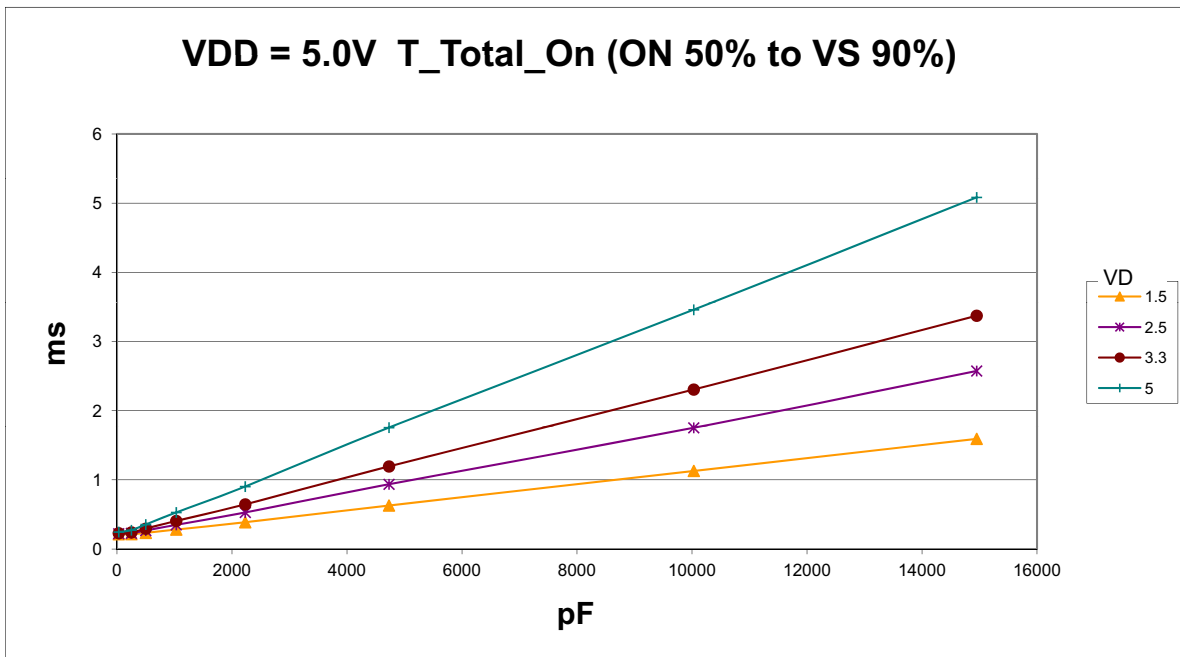
T_{Total_ON} vs. CAP @ V_{DD} = 3.3 V

SLG59M1448V T_{Total_ON}: ON (50%) - V_S (90%)
V_{DD} = 3.3 V, T_A = 25 °C. C_{LOAD} = 10 μF, I_{DS} = 100 mA



T_{Total_ON} vs. CAP @ V_{DD} = 5.0 V

SLG59M1448V T_{Total_ON}: ON (50%) - V_S (90%)
V_{DD} = 5.0 V, T_A = 25 °C. C_{LOAD} = 10 μF, I_{DS} = 100 mA





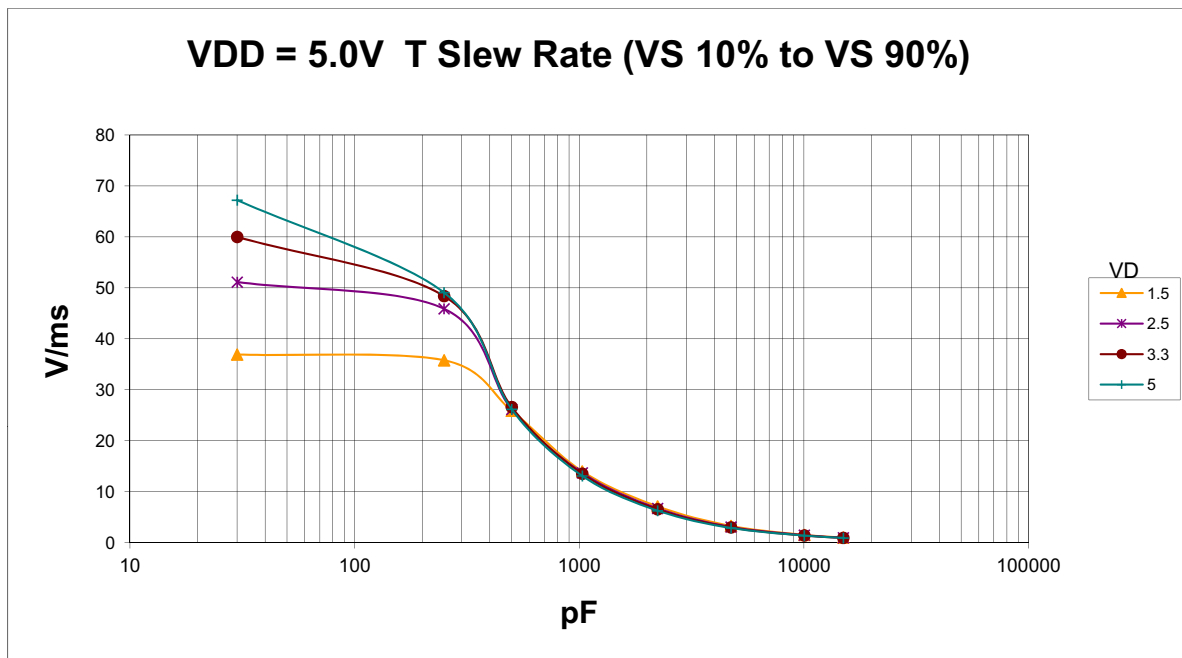
T_{SLEW} vs. CAP @ V_{DD} = 3.3 V

SLG59M1448V T_{SLEW}: V_S (10%) - V_S (90%)
V_{DD} = 3.3 V, T_A = 25 °C. C_{LOAD} = 10 μF, I_{DS} = 100 mA



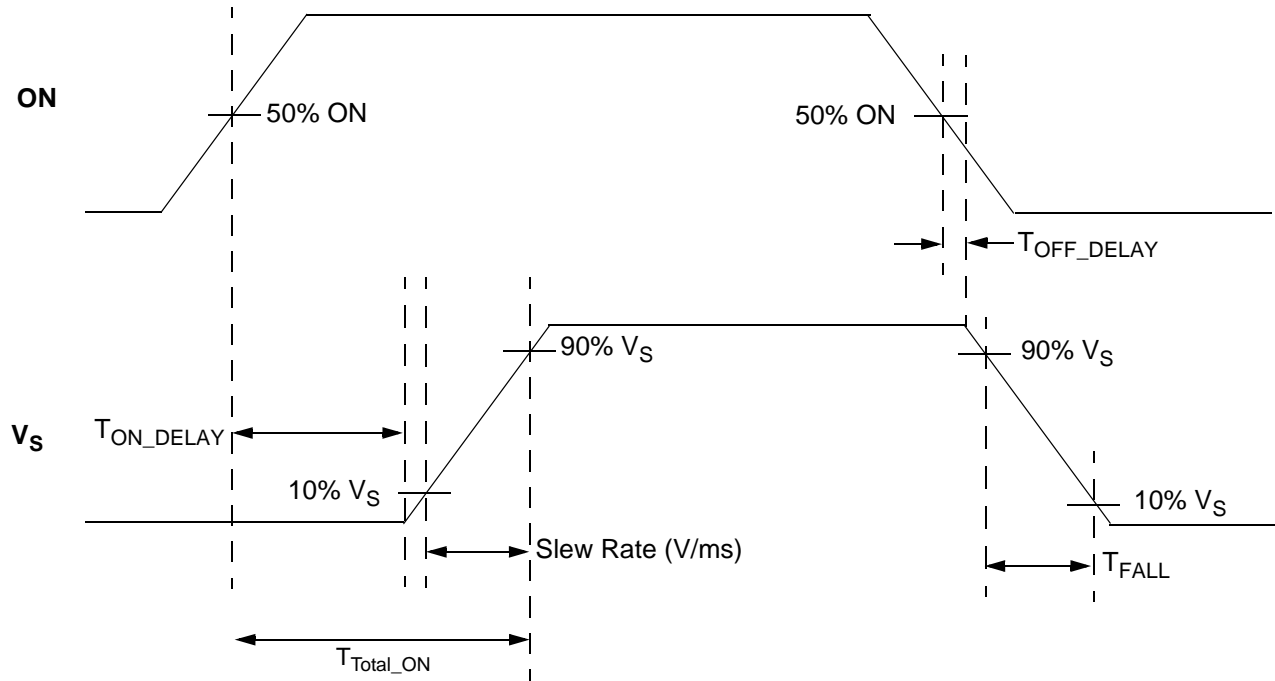
T_{SLEW} vs. CAP @ V_{DD} = 5.0 V

SLG59M1448V T_{SLEW}: V_S (10%) - V_S (90%)
V_{DD} = 5.0 V, T_A = 25 °C. C_{LOAD} = 10 μF, I_{DS} = 100 mA



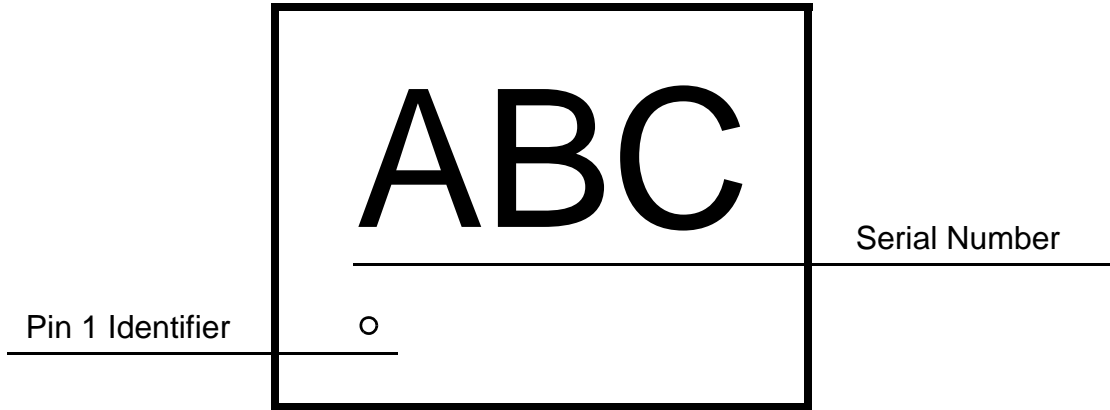


T_{Total_ON} , T_{ON_Delay} and Slew Rate Measurement





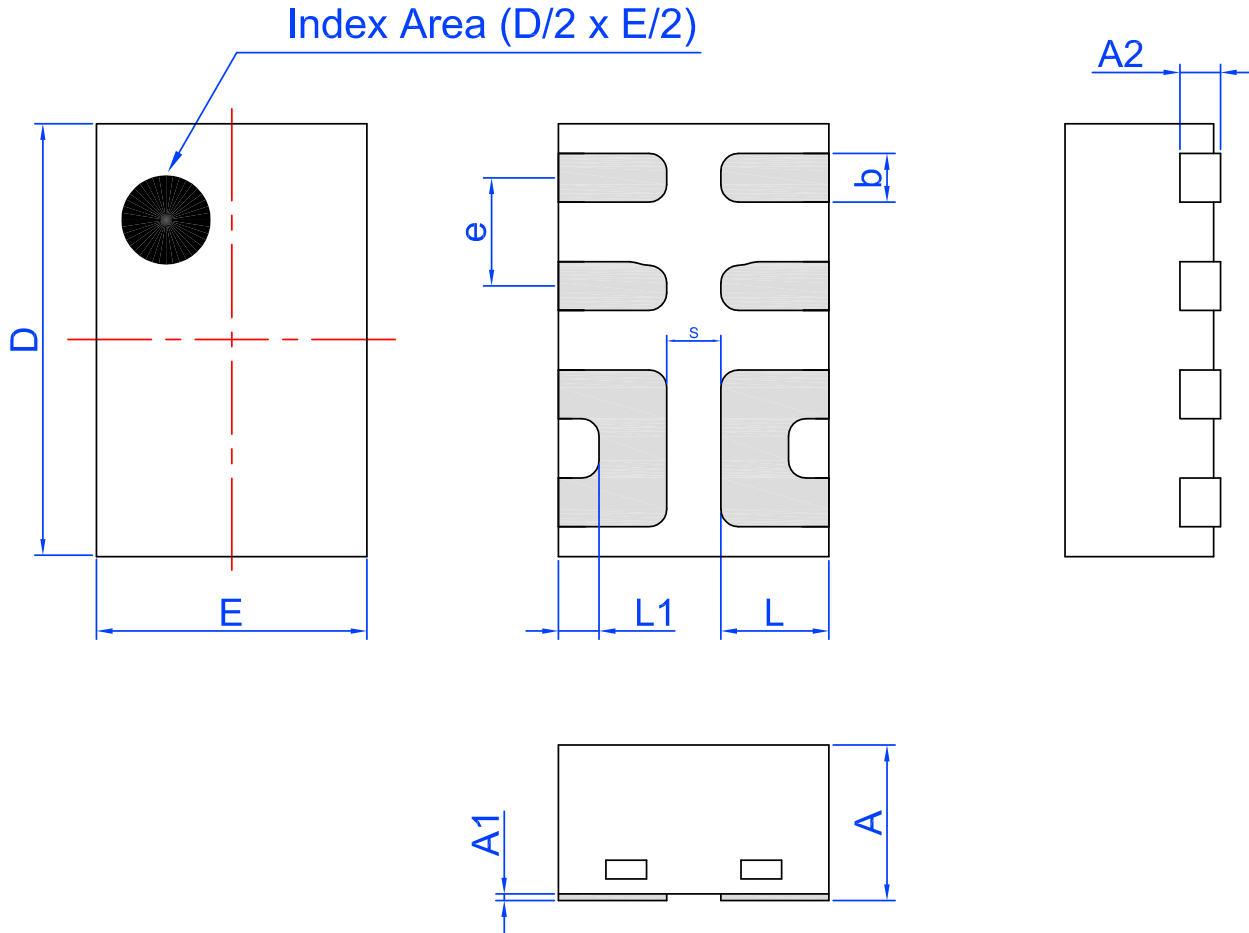
Package Top Marking System Definition





Package Drawing and Dimensions

8 Lead STDFN Package 1.0 x 1.6 mm (Fused Lead)



Unit: mm

| Symbol | Min | Nom. | Max | Symbol | Min | Nom. | Max |
|--------|----------|------|-------|--------|---------|------|------|
| A | 0.50 | 0.55 | 0.60 | D | 1.55 | 1.60 | 1.65 |
| A1 | 0.005 | - | 0.060 | E | 0.95 | 1.00 | 1.05 |
| A2 | 0.10 | 0.15 | 0.20 | L | 0.35 | 0.40 | 0.45 |
| b | 0.13 | 0.18 | 0.23 | L1 | 0.10 | 0.15 | 0.20 |
| e | 0.40 BSC | | | S | 0.2 REF | | |

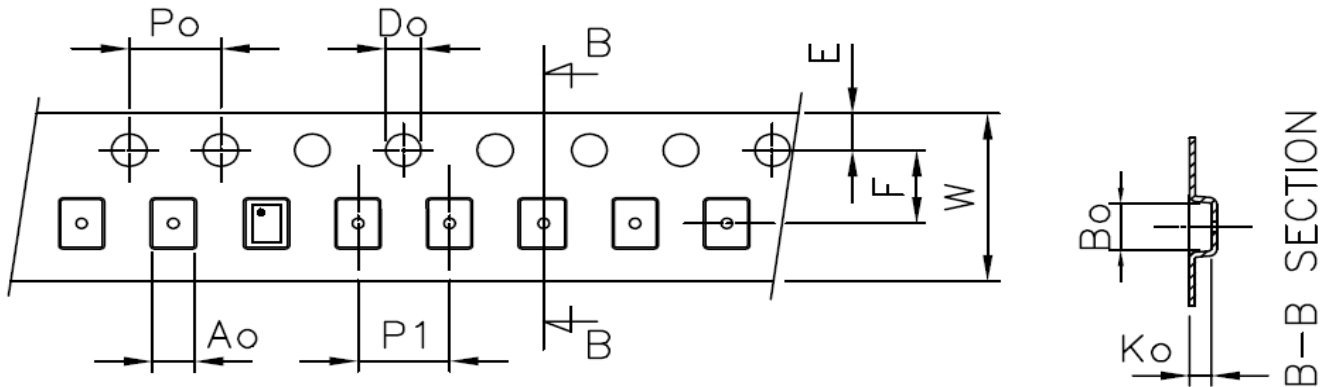


Tape and Reel Specifications

| Package Type | # of Pins | Nominal Package Size [mm] | Max Units | | Reel & Hub Size [mm] | Leader (min) | | Trailer (min) | | Tape Width [mm] | Part Pitch [mm] |
|---|-----------|---------------------------|-----------|---------|----------------------|--------------|-------------|---------------|-------------|-----------------|-----------------|
| | | | per Reel | per Box | | Pockets | Length [mm] | Pockets | Length [mm] | | |
| STDFN 8L 1x1.6mm 0.4P FC Green | 8 | 1.0 x 1.6 x 0.55 | 3,000 | 3,000 | 178 / 60 | 100 | 400 | 100 | 400 | 8 | 4 |

Carrier Tape Drawing and Dimensions

| Package Type | Pocket BTM Length | Pocket BTM Width | Pocket Depth | Index Hole Pitch | Pocket Pitch | Index Hole Diameter | Index Hole to Tape Edge | Index Hole to Pocket Center | Tape Width |
|---|-------------------|------------------|--------------|------------------|--------------|---------------------|-------------------------|-----------------------------|------------|
| | A0 | B0 | K0 | P0 | P1 | D0 | E | F | W |
| STDFN 8L 1x1.6mm 0.4P FC Green | 1.12 | 1.72 | 0.7 | 4 | 4 | 1.55 | 1.75 | 3.5 | 8 |



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.88 mm³ (nominal). More information can be found at www.jedec.org.



Revision History

| Date | Version | Change |
|-----------|---------|---|
| 8/31/2016 | 1.06 | Updated Power up/down Sequencing Considerations |
| 5/10/2016 | 1.05 | Updated Power up/down Sequence section Updated Parameter names for clarity |